METHODS FOR DEBUGGING SCAN TESTING FAILURES OF INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

The present invention is directed to a method for debugging scan testing failures of integrated circuits. The method includes identifying a bad scan path among a set of scan paths and segmenting the bad scan path into two segments. Once the bad scan path is segmented into two segments, scan tests are run to determine whether the source of errors is near the segment point. If the number of errors generated is below a threshold, the specific location of errors can be identified by tracing the errors either manually or automatically through an automated testing unit. If the source of errors is not near the segment point, the segment point is shifted based on an analysis of the errors on the good and bad scan paths. Additional scan tests are then run and the method repeated until the location of the source of errors is found.